
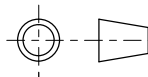


Date Draw by Verify			Modifications			IND.	
Date : 20/07/2020 Draw by :EA-ASSYTECH Checked by: M.SANGUIGNOL Project : -		Material :		Marging : +/-0.1		Nbr of layers : .	
		Finition :		Manufact.level : .		Silkscreen	
		Protection :		Scale : 2/1		TOP :... BOTTOM:...	
NXP Semiconductors 2,Esplanade Anton Philips Campus Effiscience Colombelles BP 2000 - 14906 CAEN CEDEX 9							
ASSEMBLY DRAWING TOP K32W0414A ANTENNA MODULE			SIZE A4	PCB2550-1-400		REV. 00	PL. 1/1